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Patent Application

Inventor(s): William Planey

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Examiner: D. Nguyen

Title: FLIP-CHIP PACKAGING

Form 1449**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation
	B						Yes No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
dlu	C	H. Ogiwara, M. Hayakawa, T. Nishimura and M. Nakaoka; "HIGH-FREQUENCY INDUCTION HEATING INVERTER WITH MULTI-RESONANT MODE USING NEWLY DEVELOPED NORMALLY-OFF TYPE STATIC INDUCTION TRANSISTORS"; Department of Electrical Engineering, Ashikaga Institute of Technology, Japan; Department of Electrical Engineering, Oita University, Japan; Department of Electrical Engineering, Kobe University, Japan; pages 1017-1023
	D	J. Baliga; "HIGHVOLTAGE JUNCTION-GATE FIELD EFFECT TRANSISTOR WITH RECESSED GATES"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 10; Oct. 1982
	E	J. M. C. Stork et al.; "SMALL GEOMETRY DEPLETED BASE BIPOLAR TRANSISTORS (BSIT)- VLSI DEVICES?"; IEEE Transactions on Electron Devices; Vol. ED-28; No. 11; Nov. 1981
	F	Nishizawa et al.; "ANALYSIS OF STATIC CHARACTERISTICS OF A BIPOLAR MODE SIT (BSIT)"; IEEE Transactions on Electron Devices; Vol. ED-29; No. 11; Aug. 1982
	G	Caruso et al.; "PERFORMANCE ANALYSIS OF A BIPOLAR MODE FET (BMFET) WITH NORMALLY OFF CHARACTERISTICS"; IEEE Transactions on Power Electronics; Vol. 3; No. 2; April 1988
dlu	H	Nishizawa et al.; "FIELDEFFECT TRANSISTOR VERSUS ANALOG TRANSISTOR (STATIC INDUCTION TRANSISTOR)"; IEEE Transactions on Electron Devices; Vol. ED-24; No. 4; April 1975
Examiner		Date Considered
[Signature]		07/14/05

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.